



JUN 01 2005

<p>Substitute for form 1449A/PTO</p> <p>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p><i>(use as many sheets as necessary)</i></p>				<p><i>Complete if Known</i></p>	
				Application Number	10/642,305
				Filing Date	08/18/2003
				First Named Inventor	Hongyong ZHANG et al.
				Art Unit	2811
				Examiner Name	Douglas Owens
Sheet	1	of	1	Attorney Docket Number	740756-2646

FOREIGN PATENT DOCUMENTS						
Examiner Initials ²	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Application of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁴
		Country Code ³ Number ⁴ (if known)				
DWO		JP 62-104117 A	05/14/1987	YUKI		FULL

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

Examiner Signature	/Douglas W Owens/	Date Considered	07/10/2006
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U.S. PATENT DOCUMENTS					
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DWO		US-4,059,461	11/22/1977	Fan et al.	
DWO		US-4,229,502	10/21/1980	Wu et al.	
DWO		US-4,309,225	01/05/1982	Fan et al.	
DWO		US-4,785,962	11/22/1988	Toshima	
DWO		US-4,814,292	03/21/1989	Sasaki et al.	
DWO		US-4,951,601	08/28/1990	Maydan et al.	
DWO		US-5,108,843	04/28/1992	Ohtaka et al.	
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DWO		JP 01-268064 A	10/25/1989	Hashimoto et al.	
DWO		JP 60-105216	06/10/1985	Shimizu et al.	FULL

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DWO		Mimura et al., "High Performance Low-Temperature Poly-Si n-Channel TFT's for LCD," <u>IEEE Transactions on Electron Devices</u> , Vol. 36, No. 2, pp. 351-359 (Feb. 1989)			
DWO		Ohwada, et al., "Peripheral Circuit Integrated Poly-Si TFT LCD with Gray Scale Representation", <u>IEEE Transactions on Electron Devices</u> , Vol. 36, No. 9, pp. 1923-1928 (Sept. 1989)			
DWO		Masumo et al., "Low Temperature Fabrication of Poly-Si TFT by Laser Induced Crystallization of a-Si," <u>Journal of Non-Crystalline Solids</u> , Vol. 115, pp. 147-149 (1989)			
DWO		Wright et al., "The Effect of Fluorine in Silicon Dioxide Gate Dielectrics," <u>IEEE Transactions on Electron Devices</u> , Vol. 36, No. 5, pp. 879-889 (May 1989)			

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	DWO	Wright et al., "Hot-Electron Immunity of SiO ₂ Dielectrics with Fluorine Incorporation", <u>IEEE Electron Device Letters</u> , Vol. 10, No. 8, pp. 347-348 (Aug. 1989)		
		Young & Gill, "Mobile Ion Instabilities in Polycrystalline Silicon Thin Film Transistors", <u>Applied Surface Science</u> , Vol. 39, pp. 364-367 (1989)		
		Serikawa et al., "Low-Temperature Fabrication of High-Mobility Poly-Si TFT's for Large-Area LCD's", <u>IEEE Transactions on Electron Devices</u> , Vol. 36, No. 9, pp. 1929-1933 (Sept. 1989)		
		Malhi et al., "Characteristics and Three-Dimensional Integration of MOSFET's in Small-Grain LPCVD Polycrystalline Silicon", <u>IEEE Transactions on Electron Devices</u> , Vol. ED-32, No. 2, pp. 258-281 (Feb. 1985)		
		Aritome et al., "Low-temperature nitridation of fluorinated silicon dioxide films in ammonia gas", <u>Applied Physics Letters</u> , Vol. 51, No. 13, pp. 981-983 (Sept. 28, 1987)		
		Zaima et al., "Effects of fluorine ion implantation on metal-oxide-semiconductor devices of silicon-on-sapphire", <u>Applied Physics Letters</u> , Vol. 52, No. 6, pp. 459-461 (Feb. 8, 1988)		
		Georgiev, "Electrophysical Properties of Plasma SiO ₂ Prepared from SiCl ₄ and N ₂ O", <u>Bulgarian Journal of Physics</u> , Vol. 12, No. 5, pp. 501-506 (1985)		
		Perchard et al., "Characterization of a multiple-step in-situ plasma enhanced chemical vapor deposition (PECVD) tetraethylorthosilicate (TEOS) planarization scheme for submicron manufacturing", <u>SPIE</u> , Vol. 1188, Multichamber and In-Situ Processing of Electronic, pp. 75-85 (1989)		
		Parks et al., "The Chemical Interface of Microwave Plasma Deposited SiO ₂ Films", <u>Materials Research Society</u> , Vol. 105, pp. 133-138 (1988)		
	↓	Liu et al., "Raman Characterisation of stress in Recrystallised Silicon-On Insulator", <u>Electronics Letters</u> , Vol. 24, No. 23, pp. 1420-1422 (Nov. 10, 1988)		
	DWO	Veprek et al., "Effect of Grain Boundaries on the Raman Spectra, Optical Absorption, and Elastic Light Scattering in Nanometer-Sized Crystalline Silicon", <u>Physical Review B</u> , Vol. 36, pp. 3344-3350 (Aug. 1987)		

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	DWO	Takenaka et al., "High Mobility Poly-Si Thin Film Transistors Using Solid Phase Crystallized a-Si Films Deposited by Plasma-Enhanced Chemical Vapor Deposition, <u>Japanese J. of Applied Physics</u> , Vol. 29, No. 12, pp. L2380-L2383 (Dec. 1990)			
	DWO	Sameshima et al., "XeCl Excimer Laser Annealing Used to Fabricate Poly-Si TFT's", <u>Japanese J. of Applied Physics</u> , Vol. 28, No. 10, pp. 1789-1793 (Oct. 1989)			
	DWO	Madan et al., "Use of PECVD System in Thin Film Technology", <u>Workshop on Industrial Plasma Applications</u> , pp. 1-11 (Sept. 1989)			
	DWO	Lucovsky et al., "Formation of Silicon-Based Heterostructures in Multichamber Integrated-Processing Thin-Film Deposition System", <u>Multichamber and In-Situ Processing of Electronic Materials</u> , Vol. 1188, pp. 140-150 (1989)			
	DWO	Sameshima et al., "XeCl Excimer Annealing Used in the Fabrication of Poly-Si TFT's", <u>IEEE Electron Device Letters</u> , Vol. EDL-7, No. 5, pp. 276-278 (May 1986)			
	DWO	Sera et al., "High Performance TFT's Fabricated by XeCl Excimer Laser Annealing of Hydrogenated Amorphous-Silicon Film, <u>IEEE Transactions on Electron Devices</u> , Vol. 36, No. 12, pp. 2868-2872 (Dec. 1989)			
	DWO	S. Wolf & R.N. Tauber, <u>Silicon Processing for the VLSI Era-Process Technology</u> , pp. 164-175 (1986)			
		<u>U.S. Patent Application No. 06/944,803, Mayden et al., filed December 19, 1986 (Abandoned)(Parent of U.S. Patent No. 4,951,601)</u>			

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